
Dark Souls Design Book

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Constraining Designs for Synthesis and Timing Analysis: A Practical Guide to Synopsys Design Constraints (SDC) 2013th Edition, Kindle Edition. by Sridhar Gangadharan (Author), Sanjay Churiwala (Author) › Visit Amazon's Sanjay Churiwala Page. Find all the books, read about the author, and more. See search results for this author.

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After constraining both the paths, the synthesis tool analyzes both the paths and optimizes the input path of our design with the more restrictive of the two (i.e. considering the worst-case scenario). Now let's calculate the maximum delay for combo logic-1 assuming the FF-1 has a 0.5ns setup requirement.

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STA course is designed for the working VLSI engineers who want to learn/enhance their knowledge on Synthesis and Static Timing Analysis (STA). The course will be delivered by experts in STA, who have worked on multiple tape-outs for timing closure.