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FastVDMA is an open source DMA (Direct Memory Access) controller developed at Antmicro. One of the main motivations leading to the design of an open source DMA controller was the lack of portable open source alternatives to proprietary controllers provided by FPGA vendors. This situation leads to a reduction in the reusability of DMA-based designs into different contexts when adopting multiple kinds of platforms, since DMA solutions tend to be tightly integrated with vendor-specific ...

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Abstract In this paper, the design of Direct Memory Access (DMA) Controller is proposed using Verilog. Direct memory access (DMA) is a feature of modern computers that allows certain hardware...

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If the state of the design changes after certain duration (see Fig. 7.10), then we need to add the timer in the Verilog design which are created in Listing 7.5 and Listing 7.5. For this, we need to add one more process-block which performs following actions,

7. Finite state machine — FPGA designs with Verilog and ...

Overview. The DMA controller is designed for data transfer in different system environments. Two module types : type 0 and type 1 are provided, and the user can choose the number of each module type. Type 0 modules are designed to transfer data residing on the same bus, and Type 1 modules are designed to transfer data between two different buses. Each module can support up to 4 DMA channels and the IP supports up to 16 total DMA channels.

DMA Controller - Intel

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Basicly the design is the BMD rewritten in vhdl, with working MSI and INTx interrupts, a FIFO backend for the RX and TX engines and a working linux driver for DMA. Able to achive a bandwidth of 160 MB/s Tx and 140 MB/s Rx !

DMA reference design in VHDL? - Community Forums

For any questions / remarks / suggestions / bugs please contact info@provartec.com. ----- Opencores.org project - DMA AXI This core is based on the Provartec PR200 IP - 'Generic High performance dual-core AXI DMA' The original IP is a configurable, generic AXI DMA written in RobustVerilog.

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